# RAJIV GANDHI UNIVERSITY
RONO HILLS, DOIMUKH-791112

A REPORT ON THE FACULTY DEVELOPMENT PROGRAMME

## *"Digital Signal Processing"*

**Digital Signal Processing**

**(30th April, 2018- 05th May, 2018)**

Organized By:

**Department Of Electronics and Communication Engineering,**
**Department Of Computer Science and Engineering,**
**Rajiv Gandhi University (RGU), Rono Hills, Doimukh – 791112,**
**Arunachal Pradesh, (INDIA)**
**In Collaboration with**
**E&ICT Academy, IIT Guwahati.**

## Organizing Committee

### Chief Petron

**Prof. Tamo Mibang**
Hon'ble Vice-Chancellor , RGU

### Patron(s)

**Prof. Tomo Riba**
Registrar, RGU

**Chairman**
**Prof. Utpal Bhattacharjee,**
*Dean, Faculty of Basic Science,Information Technology & Engineering Technology*
**Co-ordinators**
**Mr. Maibam Sanju Meetei,** *Asst.Prof., ECE*
**Co-coordinators**
**Mr. Ani Taggu**, *Head & Associate Prof., CSE*
**Mr. Jagdeep Rahul**, *Head & Asst. Prof., ECE*
**Mr Bhaskar Jyoti Chutia**, *Asst. Prof., CSE*
**Members**
**Ms. Champa Tanga,** *Asst.Prof. ECE*
**Mr. Kurmendra**, *Asst.Prof., ECE*
**Dr. Marpe Sora**, *Asst.Prof., CSE*
**Mr. Firos A,** *Asst.Prof., CSE*
**Ms. Bomken Kamdak Bam**, *Asst.Prof. ,CSE*
**Mr. Sikdar Md. Sultan** Askari, *Asst.Prof., CSE*
**Mr. Satish Kumar Das**, *Asst.Prof.,CSE*
**Ms. Gitanjali Choudhury**, *Asst.Prof., CSE*
**Ms. Ankita Chakraborty**, *Asst.Prof., CSE*
**Ms. Jowa Yangchin** , *Asst.Prof., CSE*
**Ms. Aditya R. Pillai**, *Asst.Prof., CSE*

## ACKNOWLEDGEMENTS

The Department of Electronics and Communication & Department of Computer Science and Engineering, Rajiv Gandhi University, We would like to expand our deepest gratitude to all members and stakeholders who have directly and indirectly guided us for organizing the Faculty Development Programme on Digital Signal Processing.

We gratefully acknowledge the encouragement, support and guidance evinced by the **Prof. Tamo Mibang, Hon'ble Vice Chancellor** of Rajiv Gandhi University and Chief Patron of the six days faculty development programme on Digital Signal Processing.

A word of special appreciation and hearty thanks are due to **Prof. Tomo Riba, Registrar**, RGU, and Patron of the programme and **Prof. Utpal Bhattacharjee**, Chairman, Dean, Faculty of Basic Sciences, IT, Engg. & Tech., A special thanks to RGU. Mr. Ani Taggu, Head, CSE, RGU and Mr. Jagdeep Rahul, Head i/c, ECE, RGU for their constant suggestion and cooperation from time to time.

We are greatly indebted to Mr. Biplav Sharma, E&ICT Academy, IIT Guwahati, Mrs. N. Kavitha, Director of STEPS Knowledge Services Pvt. Ltd. and Mr. M. Srinivasan, Assistant Engineer, STEPS Knowledge Services Pvt. Ltd. for sharing their knowledge and apprehend the technical sessions in the faculty development programme. We also thank full all the participants, faculty members, students and all the important stakeholders who contributed in organizing the programme successfully.

Mr. Maibam Sanju Meetei,
Convener,
*Asst.Prof. ECE*

## Contents

# Preface

## 1.1.About the Host Institute

### 1.1.1. The University

Rajiv Gandhi University (formerly Arunachal University) is the premier institution for higher education in the state of Arunachal Pradesh and has completed twenty five years of its existence. Late Smt. Indira Gandhi, the then Prime Minister of India, laid the foundation stone of the university on 4th February 1984 at Rono Hills, where the present campus is located. Ever since its inception, the university has been trying to achieve excellence and fulfil the objectives as envisaged in the University Act. The University got academic recognition under section 2(f) from the University Grants Commission on 28th March, 1985 and started functioning from 1st April, 1985. It got financial recognition under section 12-B of the UGC on 25th March, 1994. Since then Rajiv Gandhi University then Arunachal University has carved a niche for itself in the educational scenario of the country following its selection as a University with potential for excellence by a high level expert committee of University Grants Commission from among universities in India. The University was converted into a Central University with effect from 9th April 2007 as per notification of Ministry of Human Resource Development, Government of India.

The University is located atop Rono Hills on a picturesque tableland of 302 acres overlooking the river Dikrong. It is 6.5 km away from the National Highway 52-A and 25 km away from Itanagar, the State capital. The campus is linked with the National Highway by a Dikrong bridge. The teaching and research programmes of the University are designed with a view to play a positive role in the socio-economic and cultural development of the State. The University offers Under Graduate, Post-Graduate, M. Phil and Ph.D. programmes.

The Faculty members have been actively engaged in research activities with financial support from UGC and other funding agencies. Since inception, a number of proposals on research projects have been sanctioned by various funding agencies to the University. Departments have organized a number of Seminars, Workshops, Conferences and Webinar. Many faculty members participated in national and international conferences and seminars held within the country and abroad. Eminent scholars and distinguished personalities have visited the University and delivered lectures on various disciplines.

The academic year 2000-2001 was a year of consolidation for the University. The switch over from annual to semester system took off smoothly and the performance of the students

registered a marked improvement. Various syllabi designed by Boards of Post-Graduate Studies (BPGS) have been implemented. VSAT facility installed by the ERNET India, New Delhi under UGC-Infonet program, provides internet access.

In spite of infrastructural constraints, the University has been maintaining its academic excellence. The University has strictly adhered to the academic calendar, conducted the examinations and declared the results in time. The students from the University have found placements not only in State and Central Government Services, but also in various institutions, industries and organizations. Many students have come out successful in the National Eligibility Test (NET).Since inception, the University has made significant progress in teaching, research, innovations in curriculum development and developing infrastructure.

### 1.1.2. Departments

**Department of Electronics & Communication Engineering,** Rajiv Gandhi University, Rono Hills, Itanagar was established in the year 2015 with the aim of providing leadership in the field of Electronics & Communication Engineering and interdisciplinary research. The initiative has been taken to establish state of art research laboratories in the area of VLSI Design and Technology, MEMS and Sensors, Embedded System, Wireless Communication and Signal Processing. Department provides healthy environment to students and faculties to carry out inter department collaborative research in area like Bio medical Engineering and robotics. A team of competent and dedicated teachers are engaged in relentless pursuit of excellence in this field of engineering.

**Department of Computer Science and Engineering,** Rajiv Gandhi University, Rono Hills, Itanagarwas established in 2005, with a diploma course of one-year duration, and a three-year undergraduate course, Bachelor of Computer Application**s (BCA).** The first and second batch of the BCA programme has completed and the third batch has started from the session 2008-2009, starting from July, 2008**.** In the year 2006 the Master of Technology in Computer Science and Engineering was started in the department. The department has started the Master of Computer Application course from the session 2013-14.

### 1.2. About E&ICT Academy, IIT Guwahati

Electronics and ICT Academy is an initiative of Ministry of Electronics & Information Technology (MeitY), Govt. of India for Faculty/ Research Scholar Development Programme. Academy has planned short term training programmes on fundamental and

advanced topics in IT, Electronics & Communication, Product Design, Manufacturing with hands on training and project work. Indian Institute of Technology Guwahati, the sixth member of the IIT fraternity, was established in 1994. The academic programme of IIT Guwahati commenced in 199

### 1.3. About Six Days Faculty Development Programme.

This Faculty Development Programme was organized to learn and excel in the field of Digital Signal Processing with hardware and practical application. The experts from industries are coming to give the hands on training in various hardware kits. This programme are organized for national level.

### 1.4. Objective

This Faculty Development Programme is designed to meet the need of the engineering faculty to get a deep exposure of Digital Signal Processing which can be very well extrapolated to any application domain.

### 1.5. Expected Outcomes

The participants will be given a thorough understanding of the following topics

- Overview on Digital Signal Processing.
- Architecture and applications of C2000 based 32 bit Fixed Point DSP Engine from Texas Instruments.
- The peripherals including I/O Ports, Universal Serial Interfaces, ADC, Timers, Enhanced PWM (ePWM), Modules, On Chip Flash Access are explained and worked upon. Enhanced architectures of Floating Point Unit, Control Law Accelerator for parallel processing are also explained.
- Working with TI-RTOS to meet real time signal processing and control application requirements.

## 1.6. Resource Persons

**N.Kavitha**

Holds a Technical Director of STEPS Knowledge Services Pvt Ltd, India and handling Design and Development of Special Purpose Machines and Embedded System Development, IP related activities and Heading the Training Division catering both to Corporate and Academia on emerging technologies. *An Electronics & Communication Engineer with more than 30 years of industrial experience focused on design and development including fundamental and applied research.* Holds MS in Software Systems from BITS, Pilani, MBA in Finance, PG Diploma in IPT from NLSIU, Bangalore and DOM from IGNOU. *Speaker in various International and National conferences on topics related to Embedded Systems. Has worked extensively with Design Houses, Consultants, OEMs, Collaborators in Germany, Italy, France, Switzerland, UK, USA, Japan and Malaysia, whereby gained the experience of converting ideas to products and meeting international work practices and standards. Co-inventor in various patent applications relating to specific industrial engineering applications.* A passionate trainer to impart latest and emerging technology to the stakeholders who are in need of the same.

**M. Srinivasan**

He is an Assistant Engineer, STEPS Knowledge Services Pvt. Ltd. He has well experiences in Design and development of Embedded system with microchip and TI working with DSP and Matlab, working with IOT and application, TIRTOS, TINA TI and WEBENCH for simulation and testing, Robotics-TIRSLK and Development of RFID tag.

### 1.7. Target Population

Programme is open to Faculty Members, Research Scholars, PG & UG Students, Lab Technicians and Project Staffs from Universities, Colleges & Schools. Industry Personnel working in the concerned/allied discipline may also apply.

### 1.8. Budget (Total Expenditure)

The total expenditure of the programme was Rs. 96016.00

Advance received amount was Rs. 130000.00

Balanced amount paid by challen no. 40/15/5/018 amounting Rs. 33984.00

## Session Wise Deliberations

### 2.1 First Day

#### 2.1.1 Inaugural Sessions

The Inaugural Ceremony was started at 9.15 am on 30th April,2018.

The Prestigious part of our inauguration, **Hon'ble Vice-Chancellor i/c** of Rajiv Gandhi University, **Prof. Amitava Mitra**, in addressing the participants in the inaugural session said that the need of technology in day today life and He also stressed out digital signal processing based machines like robot can be used in various application. He also discusses the need to technology to make India one of the best technological countries in the world.

Prof. Tomo Riba, Registrar of the University talk about the story of the first computer in the Rajiv Gandhi University and shared various advantages of computer applications.

**Mrs. N. Kavitha**, Director of STEPS Knowledge Services Pvt. Ltd. She talk about various the application of Digital signal processing, advancement in technologies and future scopes of the Digital Signal Processing and its application. She also talks about many ongoing research in digital signal processing.

The First Day session was concluded by conveners of the programme Mr. Maibam Sanju Meetei

#### 2.1.2 Valedictory Session

The programme was finish after the completion of all the technical session follow valedictory session. The valedictory programme was starts at 4.30 pm, 5th May, 2018.

**Prof. Utpal Bhattacharjee, Chairman,** *Dean, Faculty of Basic Science, Information Technology & Engineering Technology*, is addressing to all the participant and talk about the needs of such programme in near future. He also appreciates the resources person and the E&ICT Academy for collaboration and for making the programme successful.

Mr. Biplav Sharma, E&ICT Academy, IIT Guwahati express the various experiences while staying in the university campus like the cleanliness and beauties of morning sunshine.

The programme was concluded with distribution of certificate and vote of thanks from Mr. Jagdeep Rahul, Head i/c, Dept. of ECE, RGU.

#### 2.1.3 Programme Schedule

**Attach at Annexure 1**

## Major Takeaways

**3.1. Academics Context:** Able to understand the Digital Signal Processing, its application and various advancement in Digital Signal Processing. Provide the hands on training on hardware kits for application of digital signal processing. Discussed various parameter while choosing the hardware.

**3.2. Research Context:** Able to implement the interfacing with analog inputs and process the data with various hardware. Able to work on various IDE for different hardware.

**3.3. Future Scope:** Digital Signal Processing going to provide many scope in the field of medical, vehicles and etc.

The demand for Digital signal processing certified professionals will grow along with the developments in IOT and Artificial Intelligence. Gaining a certificate in Digital Signal will give you an edge over other IT professionals.

# Annexure 1: Programme Schedule

## Faculty Development Digital Signal Processing

Venue: **Rajiv Gandhi University, Itanagar**

**(30April – 05 May, 2018)**

| Date | Time | Topic |
|---|---|---|
| Day-1 30-04-2018 | 08:45am-09:15am | Registration and Reporting |
| | 09:15am-09:45am | Inauguration |
| | 09:45am-10:00am | Tea Break |
| | 10:00am-01:00pm | **Module 1** - Overview on Digital Signal Processing and its applications. TI Portfolio. Architecture of DSP and its peripherals |
| | 01:00pm-01:30pm | Lunch Break |
| | 01:30pm-01:45pm | **Hands on** experience on Hardware Creating first project with CCS IDE and working with IO Ports |
| | 01:45pm-03:45pm | **Hands on** experience on Peripheral – I/O Port and Interrupts, Timers and PWM |
| | 03:45pm-04:00pm | Tea Break |
| | 04:00pm-5:00pm | Working with Peripheral – ADC. |
| | 05:00pm-05:30pm | MCQ |
| Day-2 01-05-2018 | 09:30am-11:00am | **Module2:** Working with Serial Communication Interface(SCI) peripheral – UART / USB |
| | 11:00am-11:15am | Tea Break |
| | 11:15am-01:15pm | **Module 3:** Introduction to Energia IDE : Working with Digital IO & Analog |
| | 01:15pm-01:45pm | Lunch Break |
| | 01:45pm-03:45pm | **Module 4:** Working with Experimenter board |
| | 03:45pm-04:00pm | Tea Break |
| | 04:00pm-05:00pm | **Module 5:** Peripheral –I/O Port with LCD Interface and Matrix Keypad |
| | 05:00pm-5:30 pm | MCQ |
| Day-3 02-05-2018 | 09:30am-11:00am | **Hands on** experience :Introduction to TI-RTOS. Need for TI-RTOS in Digital Signal Processing Applications |
| | 11:00am-11:15am | Tea Break |
| | 11:15am-01:15pm | **Module 6:**Working with TI-RTOS |
| | 01:15pm-01:45pm | Lunch Break |
| | 01:45pm-3:45pm | Working with TI-RTOS contd… |
| | 03:45pm-04:00pm | Tea Break |
| | 04:00pm-05:00pm | Working with TI-RTOS contd… |
| | 5:00pm-05:30pm | MCQ |

| | | |
|---|---|---|
| Day-4<br>03-05-2018 | 09:30am-11:00am | **Module 7:** Advanced Concepts of Signal processing - Viterbi, Complex Math and CRC |
| | 11:00am-11:15am | Tea Break |
| | 11:15am-01:15pm | **Module 8:** Parallel Processing with Control law Accelerators for Complex and Real Time Signal Processing |
| | 01:15pm-01:45pm | Lunch Break |
| | 01:45pm-03:45pm | **Demonstration:** Working/Demo with MATLAB Simulink and Embedded Coder- IO Ports, ADC, Serial Interface PWM Generation |
| | 03:45pm-04:00pm | Tea Break |
| | 04:00pm-05:00pm | **Demonstration:** Working/Demo with MATLAB script for an off-line Low Pass and test the filter using the samples acquired from ADC from hardware. |
| | 05:00pm-05:30pm | MCQ |
| Day-5<br>04-05-2018 | 09:30am-11:00am | **Module 9:** Introduction to TMS320C6748 DSP Development Kit and its Peripherals. Applications with Audio Processing and Signal Analysis |
| | 11:00am-11:15am | Tea Break |
| | 11:15am-01:15pm | **Hands on** with Fixed Point vs Floating Point DSPs. Floating Point Notation and Exercises |
| | 01:15pm-01:45pm | Lunch Break |
| | 01:45pm-03:45pm | **Hands on** with Demo of Linear and Circular Convolution in TMS320C6748 |
| | 03:45pm-04:00pm | Tea Break |
| | 04:00pm-05:00pm | **Hands on** with Demo of Waveform Generation using TMS320C6748 and Implementation of Filters using TMS320C6748 |
| | 05:00pm-05:30pm | MCQ |
| Day-6<br>05-05-2018 | 09:30am-11:00am | **Project** |
| | 11:00am-11:15am | Tea Break |
| | 11:15am-01:15pm | Project contd… |
| | 01:15pm-01:45pm | Lunch Break |
| | 01:45pm-03:45pm | **Project completion followed by Evaluation.** |
| | 03:45pm-04:00pm | Tea Break |
| | 04:00pm-04:30pm | MCQ |
| | 04:30pm-05:00pm | Closing ceremony and Certificate Distribution |

# Annexure 2: List of Participants

## Faculty Development Programme on "Digital Signal Processing"

REPORTING LIST

Date:30April-05May 2018

Venue: Rajiv Gandhi University, Itanagar

| SlNo. | Name of Participants (Use Block Letters) | Gender | Designation | Category | Name & Address of the Organization/Institute/College | Phone/Mobile No. | Transaction Details with Date | Remarks | Signature |
|---|---|---|---|---|---|---|---|---|---|
| 1 | MAIBAM SANJU MEETEI | Male | Assistant Professor | OBC | Rajiv Gandhi University | 9436069533 | | Id Submitted | |
| 2 | ADITYA R PILLAI | Female | Assistant Professor | UR | RGU,RONO HILLS,DOIMUKH | 9495972270 | | ID submitted 01/05/18 | |
| 3 | KURMENDRA | Male | Assistant Professor | UR | Rajiv Gandhi University, Doimukh | 8415912663 | | ID Submitted 01/05/18 | |
| 4 | ANKITA CHAKRABORTY | Female | Assistant Professor | UR | Rajiv Gandhi University | 8822715781 | " | ID submitted on 01/05/18 | |
| 5 | ABHIJIT BISWAS | Male | Assistant Professor | SC | ASSAM UNIVERSITY | 9435173520 | 201804163855731 7 | Documents OK | |
| 6 | CHAMPA TANGA | Female | Assistant Professor | ST | Rajiv Gandhi University DOIMUKH | 9862060147 | | Id Submitted | |
| 7 | FIROS A | Male | Asst. Professor | UR | Rajiv gandhi University doimukh | 9402212509 | | | |
| 8 | MARPE SORA | Male | Assistant Professor | ST | Cse | 9436896346 | | ID Submitted on 04/05/18 | |
| 9 | JOWA YANGCHIN | Female | Assistant Professor | ST | Rajiv Gandhi University | 9862198653 | | ID Submitted 01/05/18 | |
| 10 | SATISH KUMAR DAS | Male | Assistant Professor | SC | Rajiv Gandhi University | 8413838038 | | ID Submitted 01/05/18 | |
| 11 | JAGDEEP RAHUL | Male | Assistant Professor | SC | Rajiv Gandhi University | 70857579756 | | ID Submitted 01/05/18 | |
| 12 | BHASKAR JYOTI CHUTIA | Male | Assistant Professor | UR | Rajiv Gandhi University | 9707628378 | | ID Submitted 02/05/18 | |
| 13 | BOMKEN KAMDAK BAM | Female | Assistant Professor | ST | Rgu | 9436047555 | | | |
| 14 | SIKDAR MD SUTAN ASKARI | Male | Assistant Professor | UR | Rajiv Gandhi University | 8413838031 | | | |
| 15 | GEETANJALI CHOUDHURY | Female | Assistant Professor | UR | DEPT OF COMPUTER SCIENCE AND ENGINEERING RAJIV GANDHI UNIVERSITY | 9707766806 | | | |
| 16 | YABOM YUTO | Female | Student | ST | RAGIV GANDHI UNIVERSITY DOIMUKH | 8414801267 | | ID Submitted 02/05/18 | |


## Faculty Development Programme on "Digital Signal Processing"

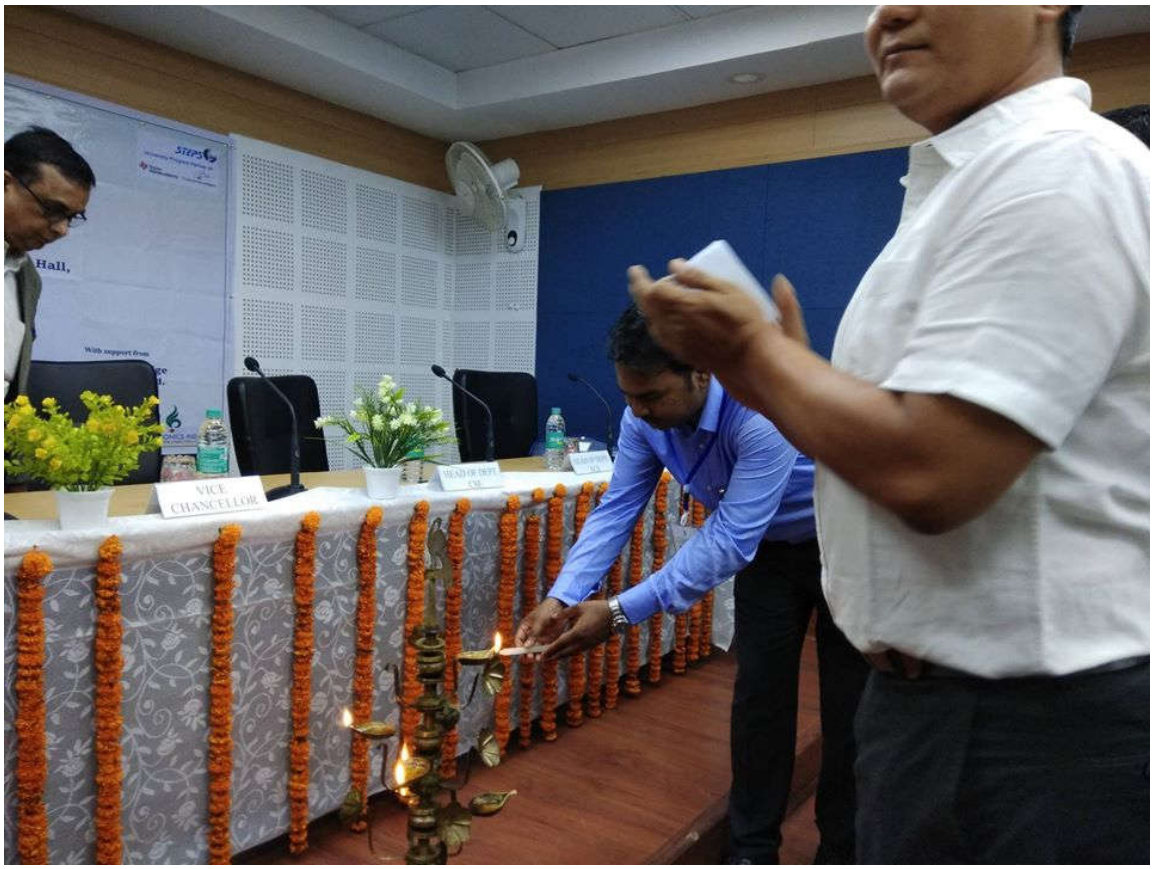
REPORTING LIST

Date:30April-05May 2018

Venue: Rajiv Gandhi University, Itanagar


| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 17 | ANIL CHAMUAH | Male | Student | OBC | Dept. of ECE, RGU | 8794498141 | | ID OK | |
| 18 | AMAR BAHADUR BISWAKARMA | Male | Student | OBC | RAJIV GANDHI UNIVERSITY(RGU) | 8794685820 | | ID ok | |
| 19 | SATISH KUMAR DAS | Male | Assistant Professor | SC | Deptt. Of CSE, R.G.U | 8413838038 | Multiple Entry | | |
| 20 | CHOW MALAPAN KHAMHOO | Male | Student | ST | Dept. of ECE, RGU | 7005290547 | | ID OK | |
| 21 | KABITA KUMARI | Female | Student | OBC | RGU, RONO HILLS | 8837303319 | | ID ok | |
| 22 | NANG ANIJA MANLONG | Female | Student | ST | RAJIV GANDHI UNIVERSITY RONO HILLS DOIMUKH | 7085595314 | | ID OK | |
| 23 | L BOBINSON SINGHA | Male | Student | OBC | RGU RONO HILLS DOIMUKH | 9435398696 | | ID ok | |
| 24 | SHIVNATH RAI | Male | Student | OBC | RGU Doimukh | 7654175121 | | ID OK | |
| 25 | ANIL KUMAR SHAW | Male | Scientist-C | UR | NIELIT Itanagar | 9863429681 | Transaction detail Submitted on 04/05/18 | ID proof submitted on 04/05/18 | |
| 26 | MRINAL JYOTI SARNA | Male | Research Scholar | UR | RGU | 98647 86669 | | ID Submitted | |
| | | | | | | | | | |
| 27. | SHASHANK AWASTHI | MALE | Research Scholar | UR | NERIST | 8787751105 | | ID Submitted on 05/05/18 (transaction mail) | |
| 28 | SHRISTY KK SHARMA | MALE | STUDENT | UR | RGU | 8259971263 | | ID submitted on 01/05/18 | |
| 29. | Uthar Kumar | MALE | STUDENT | UR | RGU | 8794243471 | | On Spot ID OK | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |

# Annexure 3: Photographs (if any)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ON
DIGITAL SIGNAL PROCESSING
(30 April – 05 May, 2018)
Venue
Institute of Distance Learning, Conference Hall,
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Organised by
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ELOPMENT PROGRAMME
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